Design and Transistor-Level Simulation of a High-Order Gm-C Filter Bank

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***Abstract*—This paper describes the overall design of a Gm-C filter bank devised to analyze supraharmonic components, which are signals with frequencies from 2 to 150 kHz superimposed to the electric grid voltage signal. The bank is composed by ten elliptic filters with different frequency bands. The design of the operational transconductance amplifiers (OTAs) especially conceived to achieve high linearity and low transconductance values, as well as the strategy conceived for biasing and tuning a large number of OTAs, are discussed. Finally, the transistor-level AC simulation results comparing the frequency response of one transistor-based filter with other filters responses for the same range are shown.**

Keywords—supraharmonics, analog filter bank, Gm-C filters, operational transconductance amplifiers.

I. INTRODUCTION

Power quality distortions are object of growing studies in the past years. The electrical power signal distortions in the range of 2 kHz to 150 kHz are called supraharmonics, and their relevance in the past years are due to their main causes, like inverters that employ Pulse Width Modulation (PWM) for power conversion, and their interaction with other kind of devices, like power line communications (PLC) modems [1-2].

In a previous work [3], a high-order analog filter bank was proposed in order to apply subsampling and other digital signal processing techniques to reduce the amount of data and the computational burden of the calculation of the supraharmonics components by applying the Fast Fourier Transform (FFT).

That work proposed a Gm-C filter bank, based on the operational transconductance amplifiers (OTAs) and capacitors, especially due to their tunability. The Gm-C filter would replace a original passive filter bank conceived to the proposed application, in [4], with advantages, like a higher attenuation in the rejection band.

It was shown that the desired transfer function should require an elliptic, 16th-order band-pass filter. Each filter was composed by an arrangement of eight blocks of second-order Gm-C filters. For implementation of the elliptic transfer function, a cascade of non-canonical second-order sections was adopted, each composed by nine OTAs.

However, the results shown in [3] are for simplified OTAs, where each OTA is modeled by a voltage-controlled current source in parallel with a high output impedance. Each filter is composed by

$$8\ sections\ x\ 9\ OTAs/section = 72\ OTAs \quad (1)$$

Considering that the proposed bank is constituted by ten filters, with 15 kHz of band (exception for the filter 1, which ranges from 2 to 15 kHz), there will be an amount of 720 OTAs in the circuit. If one considers that the OTA transconductance can be adjusted by its biasing current, it would be impractical that each OTA could have one external current biasing input. Even assuming that many of the filter OTAs are equal, letting that one external current can be replicated in order to bias several of them, it remains quite difficult to use external resistors to produce a biasing current, which would require too many pins of a chip.

Moreover, the transistor-level design of an OTA with low transconductances and high linearity is not trivial, and not uniquely dependent of the biasing current, as it will be shown.

This paper describes the overall design of the high-order Gm-C filter bank, including a description, at system-level, of a mixed-signal circuit devised to adjust the transconductances of a large number of OTAs to be integrated into a single chip. The transistor-level SPICE AC simulation results obtained for one of the filters, designed at a hypothetical 180 nm CMOS process, are shown and compared to the output of other filters designed for the same range.

The paper is organized as follows: in the Section II, the structure of the circuit is shown, as well as the discussion about the biasing circuitry. In Section III, the simulation results are discussed. Finally, the conclusions are presented in Section IV.

II. SYSTEM DESCRIPTION

The system is composed by ten passband filters. Each filter is the cascading of eight second-order filters, as illustrated in Fig. 1, leading to a 16th-order transfer function. Different topologies presented in the literature have been evaluated and the topology that had better results was the one introduced in [5]. This structure is called follow-the-leader-feedback (FLF) Gm-C filter. A second-order FLF filter structure is shown in Fig. 2. It is composed by two Gm-C integrators, a feedback

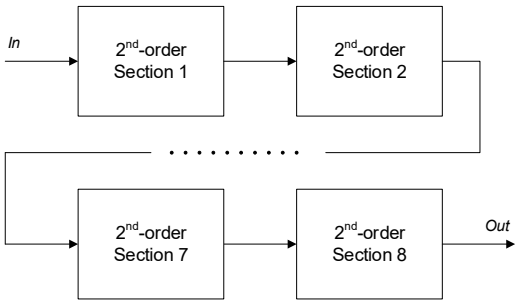

Fig. 1. Cascade of eight second-order sections.

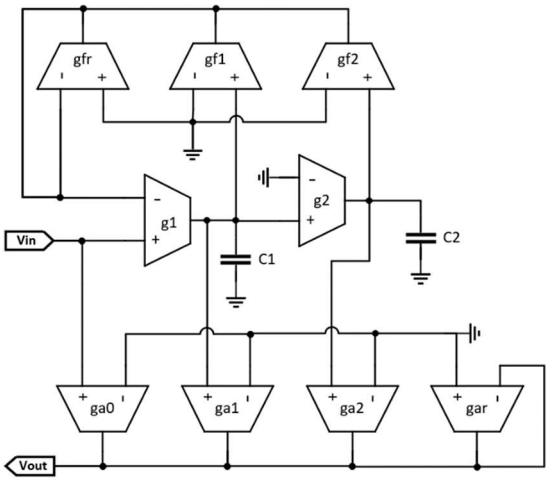

Fig. 2. A second-order FLF Gm-C filter section.

network (upper part) and a feedforward output summation network (lower part).

Although it is a non-canonical structure, with a higher number of OTAs than it is present in other topologies [6], this circuit has some advantages, as more degrees of freedom for design. This is necessary to implement the transfer functions of the elliptical filters. Moreover, the FLF filter has only grounded capacitors and has the possibility of achieving a zero capacitor spread, which is interesting for an integrated implementation of a high-order filter.

The transconductances calculation methodology is well explained in [3], and a complete set of values for each filter can be found in [7]. In calculation, some element values shown in Fig. 2 needed to be arbitrated, like C_1, C_2, g_1, g_2, g_{ar}, and g_{fr}.

However, it was noted that some transconductance values were quite small, requiring special techniques for producing very-low transconductance amplifiers, as those related in [8]. Moreover, from simulation, it is found that the desired transfer function would be achieved only for OTAs with output impedances of order of 1 GΩ, further degrading for lower values. The values were then recalculated, arbitrating higher values for C_1 and C_2 (10 pF, instead of 1 pF). Table I shows, as example, the achieved values for one of the filters, for the 45 – 60 kHz frequency band. The complete set of recalculated values are in [9]. An output impedance of 100 MΩ was assumed for all of the new transconductances used to simulate the filters, which is a more realistic assumption.

From a chip area perspective, the capacitors occupy a significative part of the die. In modern submicrometer processes, it is possible to achieve, by using metal-insulator-metal (MIM) capacitors, a capacitance per area equal to, at minimum, 1.0 fF/μm^2 [10]. For this case, a 10-pF capacitor would have an estimate area of 10x10^3 μm^2 = 0.01 mm^2.

TABLE I. PARAMETERS FOR THE 45–60 KHZ BANDPASS FILTER (RECALCULATED).

Section	Transconductances (in μA/V)					
	g_1	g_2	g_{f1}	g_{f2}	g_{a1}	g_{a2}
S1	0.1	1	0.789	1420	-0.413	-510
S2	0.1	1	3.90	1410	-2.04	592
S3	0.1	1	13.1	1350	-6.85	110
S4	0.1	1	28.5	1180	-14.9	143
S5	0.1	1	25.6	959	-13.4	250
S6	0.1	1	10.4	843	-5.42	-59.2
S7	0.1	1	2.96	808	-1.55	-14.9
S8	0.1	1	0.592	800	-0.310	-4.70
For all sections			g_{a0} = 5.23 μA/V $g_{ar} = g_{fr}$ =10 μA/V $C_1 = C_2$ = 10 pF			

Assuming that 16 capacitors of 10 pF will be used in each filter and neglecting the necessary spacing between capacitor plates, the total area for the capacitors employed in the bank will be approximately 1.6 mm^2.

The transistor-level implementation of the OTAs is described as follows, as well as the approach for their biasing and tuning.

A. OTA structure

The proposed topology for designing the OTA is based on the source-degeneration scheme, that can linearize the OTA response and either reduce its transconductance gain, if compared to the basic OTA [11].

The circuit is depicted in Fig. 3. Each transistor of the differential pair (M_1 and M_2) is biased by currents I_{B1} and I_{B2}, imposed by transistors M_{B1} and M_{B2}, respectively (replied from I_B, which flows into M_B). It is intended that I_B can be generated by a 5-bit output current digital-to-analog (D/A) converter.

A resistor R_1 is then placed among the sources of M_1 and M_2. The resistor can be replaced by MOSFETs in triode region, acting as voltage-controlled resistors [12]. The presence of cascode stages in the circuit, properly biased at V_{B1} and V_{B2}, increase the output impedance, a required feature for the OTAs to be used in this project.

From [12], it can be demonstrated that the transconductance gain, G_m, is given by

$$G_m \cong \frac{g_m}{1+g_m.R_1} . \quad (2)$$

Considering that g_m is the transconductance of M_1 (or M_2), given by

$$g_m = \sqrt{2k'_n \left(\frac{W}{L}\right)_1 I_{B1}} . \quad (3)$$

Where k'_n is the process transconductance parameter, $(W/L)_1$ is the aspect ratio of M_1 and I_{B1} is the biasing current

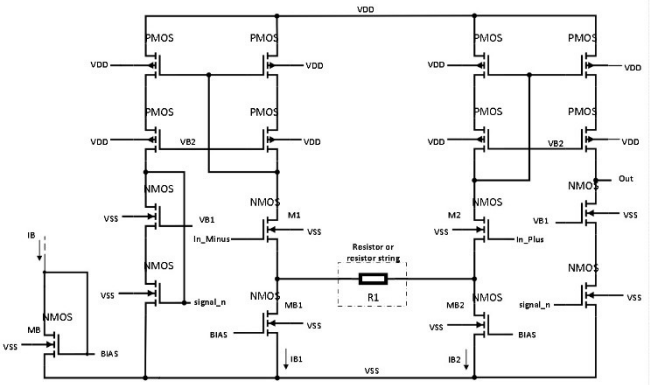

Fig. 3. The proposed OTA, with the source-degeneration scheme.

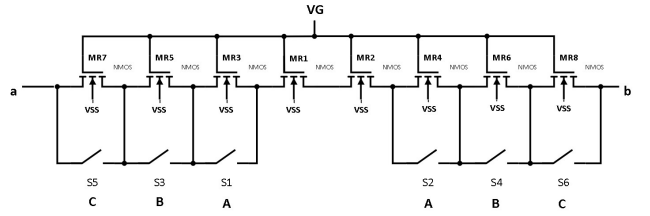

Fig. 4. Detail on the resistive string, imlemented by MOSFETs in triode region.

of M_1. M_1 and M_2 are matched elements, so that $g_m = g_{m1} = g_{m2}$.

For the proposed application, the resistor R_1 is intended to be implemented by a resistive string, where the resistor elements are replaced by N-channel MOSFETs in triode region, as it is shown in Fig. 4. The total resistance between nodes S_1 and S_2 can be adjusted into discrete values by controlling the state of the analog switches by external logic signals. In practice, the switches are also implemented by N-channel MOSFETs, with minimum length.

The gate voltage, V_G, is kept constant for all the OTAs. The option for controlling the resistance by the switches, instead of adjusting V_G, is that a large number of OTAs is required, and it could be impractical to control V_G for each OTA individually. According to (2) and (3), by adjusting the string resistance, combined with the control of the biasing current, it is possible to reach the expected OTA transconductance.

B. Biasing and tuning circuit

Considering that the OTA transconductance, G_m, can be adjusted by setting g_m (proportional to the square root of I_B) and R_1, then I_B and R_1 are parameters to be externally controlled in order to tune the filters (assuming that V_G is a fixed value).

The biasing and setting of a large amount of OTAs represent a big challenge in this study. The bias/tuning circuit was planned at system level using basic logic blocks in order to configure the registers that store the digital values that will be used by the current output D/A converters to perform the biasing.

According to Fig. 5, the biasing/tuning structure is composed of a control circuit (state machine associated with a counter), shift registers, parallel-in-parallel-out (PIPO) registers and decoders.

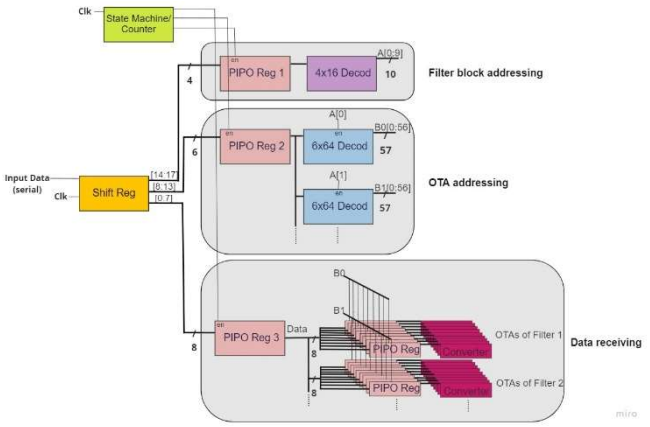

Fig. 5. Biasing/tuning block diagram.

The data writing operation is performed by the control circuit, which coordinates the enabling of the PIPO registers that receive the input data. This configuration is done by a mod-24 counter that composes an autonomous state machine.

The input data is received serially by a shift register. The counter increments accordingly to the input clock cycles. Depending on the counter value, the data is redirected to the filter block addressing, OTA addressing or data receiving sub-systems, as indicated in Fig. 5.

The data transferred to the system are composed of three bytes (24 bits). The first eight bits are the OTA configuration data, which can be divided into five bits to be written to the input of the D/A converters, and three bits that configure the switches of the resistive string depicted in Fig. 4.

The next six bits are related to the decoder value that addresses a specific OTAs within a filter. It is important to emphasize that some of the 72 OTAs (in each filter block) have identical characteristics and configurations. Then, the data for 57 OTAs have to be stored (some are replicated for more than one OTA), so that a 6-to-64-line decoder can be used.

The next four bits are related to the address of one of the ten filters present in the complete circuit, and the remaining six bits are reserved to facilitate a future implementation of serial communication with an external microcontroller.

III. Simulation Results

The filter bank was simulated in LTSpice XVII using MOSFETs BSIM3 predictive models for 180 nm node (1.8 V), available in [13]. For the circuit, V_{DD} = +0.9 V and V_{SS} = –0.9 V. The AC sweep simulation was done in LTSpice XVII using the aforementioned models. Components values can be found in [9].

For simulation, some simplifications were made, as follows: *(i)* the string composed by various MOSFETs, as depicted in Fig. 4, was not adopted, being replaced by just one N-channel MOSFETs in triode region (or two in series, depending on the required resistance), with V_G = 0.9 V; *(ii)* exact values for I_B were used, instead of quantized values, which will be actually used in a practical implementation, considering that the current will flow from a D/A converter; *(iii)* the active loads, which in circuit of Fig. 2 are implemented by OTAs g_{fr} and g_{ar}, were replaced by passive

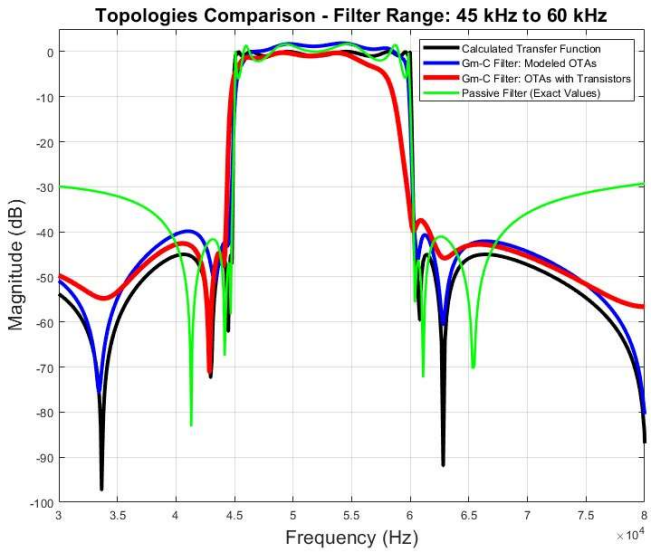

Fig. 6. Comparison of different responses for the 45-60 kHz filters.

elements (resistors), with values equal to the inverse of the transconductances.

This last simplification was made because some adjusts were necessary on the values of these elements to better fit the sections frequency response curves with the ideal ones. It is probably related to the output impedance of the OTAs of the feedback or the feedforward output summation network, and will be investigated in future.

The results for the filter designed for the 45-60 kHz range are shown in Fig. 6. The graphs compare the response of the transistor-based circuit with the responses of the filter composed by modeled transconductances (with recalculated values, shown in Table I), the theoretical (ideal) filter and the passive filter designed for the same range, simulated with exact values for the components (as shown in [3]).

It can be observed that the response for the transistor-level simulated Gm-C filter has a lower attenuation over stopbands, if compared with the ideal response. However, it has a higher attenuation over stopbands (above 10 dB), if compared with the passive filter. Considering that the integrated circuit implementation could lead to a considerable area reduction, compared to the passive filter, the active Gm-C filter represents an interesting choice for the desired application.

IV. Conclusion

This paper presented the overall design of a Gm-C bank filter for supraharmonic analysis. Starting from the recalculated values for simplified, modeled transconductances, willing to eliminate very low values, the work presented the general structure of the OTA to be used to implement the circuit depicted in Fig. 2. A source-degeneration scheme, shown in Fig. 3, can either reduce the transconductances and increase linearity of the OTAs.

For a future chip implementation of the filter bank, the biasing/tuning scheme for a large amount of OTAs (720 at total) represent a challenge, and a possible system-level strategy was discussed briefly in Section II-B.

Transistor-level AC simulation of one of the filters shows that the frequency response can approximate the theoretical curve, exhibiting a slightly lower attenuation at the stopbands, but considerably higher than that presented by a passive filter.

The study on the combined OTAs output impedances, in order to better adjust the filter responses, the design of the current-mode D/A converter and the design of the biasing/tuning system using the Verilog hardware description language are considered for future works, which will contribute for an effective chip implementation of the filter bank on a standard, commercial CMOS process.

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